WHAT IS CLAIMED IS:

1. A correlator for determining a phase difference between a received spreading code included in a spread spectrum signal and a reference code, comprising:

a reference spreading code generator for generating the reference spreading code;

a combined code generator for generating a combined spreading code form the reference spreading code; and

arithmetic circuit for calculating a correlation between the received spreading code and the combined spreading code.

2. The correlator of claim 1, wherein the combined code generator combines a plurality of weighted and phase shifted occurrences of the reference spreading code.

3. The correlator of claim 1, wherein arithmetic circuit includes a multiplier for multiplying the received spreading code with the combined spreading code, and an integrator for integrating an output of the multiplier.

4. The correlator of claim 1, which further includes a phase detector for detecting the phase difference based upon an output of the arithmetic circuit .

5. The correlator of claim 1, which further includes a weight selector for changing the weighting of the plurality of occurrences of the reference spreading code.

6. A correlator for determining a phase difference between a received spreading code included in a spread-spectrum signal and a reference spread code comprising:

a reference spreading code generator for generating the reference spread code;

a first combined code generator for generating a first combined code from the reference spread code;

a first arithmetic circuit for calculating a first correlation between the received spread code and the first combined code;

a second combined code generator for generating a second combined code from the reference spread code;

a second arithmetic circuit for calculating a second correlation between the received spread code and the second combined code; and

a third arithmetic circuit for determining the phase difference based on the first and second correlations.

7. The correlator of claim 6, wherein the third arithmetic circuit divides the first correlation by the second correlation.

8. The correlator according to claim 6, wherein the first combined code generator applies first weighting to a plurality of phase-shifted occurrences of the reference spreading code on the basis of values obtained by sampling one period of a sine-wave signal in units in which the phase shift is performed and then combining the plurality of phase-shifted occurrences of the reference spreading code after being weighted.

9. The correlator of claim 6, wherein the second combined code generator applies second weighting to a plurality of phase-shifted occurrences of the spreading codes on the basis of values obtained by sampling one period of a cosine-wave signal in units in which said phase shift is performed and then combining the plurality of phase-shifted occurrences of the references spreading code after being weighted.

10. The correlator of claim 6, wherein the first arithmetic circuit includes:

a multiplier for multiplying the received spreading code and the first combined spreading code;

integrator for integrating an output of the multiplier to produce the first correlation.

11. The correlator of claim 6, wherein the second arithmetic circuit includes:

a multiplier for multiplying the received spreading code and the second combined spreading code;

an integrator for integrating an output of the multiplier to provide the second correlation.

12. The correlator of claim 6, which further includes a sliding correlator for discriminating on the bases of the phase difference, a phase area in which a true phase difference between received spreading code and the reference code resides, and searching within the phase area sequentially to find a phase for which correlation is maximized.

13. A delay locked loop circuit for maintaining phase synchronization between a received spreading code included in a spread-spectrum signal and a reference spreading code, comprising:

a reference spreading code generator for generating the reference spreading code;

a combined code generator for generating a combined spread code from the reference spreading code;

arithmetic means for detecting a phase difference between the received spread code and the reference spread code using the combined spreading code; and

voltage controlled oscillator for controlling a phase of the reference spreading code on the basis of the phase difference.

14. The delay locked loop circuit of claim 13, wherein the arithmetic means includes a multiplier for multiplying the received spreading code by the combined spreading code, and filter for filtering an output of the multiplier.

15. The delay locked loop circuit of claim 13, wherein the combined code generates first weights and then combines a plurality of phase shifted occurrences of the reference spreading code.

16. The delay locked loop circuit of claim 15, wherein the combined code generator makes positive, and successively reduces in magnitude, the weights of n-

number of reference spreading codes of small phase shift constituting a first half of 2n-(where n is a positive integer) number of reference spreading codes that have been successively shifted in phase, and makes negative, and successively increases in magnitude, the weights of n-number of reference spreading codes of large phase shift constituting a second half of the reference spreading codes that have been successively shifted in phase.

17. The delay locked loop circuit of claim 16, wherein a plurality of weights for which the n is different, outputting the combined spreading code using a weight for which n is large, and outputting a combined spreading code using the weight for which n is small whenever the phase difference falls below a set value.